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7. (Amended) The method of claim 1 and further comprising fabricating a second gate region within the memory circuit.

26. (Amended) A method of forming a non-volatile electrically alterable semiconductor FLASH memory cell having a programming operation and an erase operation, with reduced, random, single bit data loss in a memory circuit comprising:

providing a silicon substrate;

heating the silicon substrate in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the silicon substrate;

fabricating a field oxide region and a channel region over or within the silicon substrate;

heating the silicon substrate with the field oxide region and channel region in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the layer;

growing an oxide over the channel region in an atmosphere enriched in Hydrogen isotope;

fabricating at least one gate member; and

passivating the memory cell having a programming operation and an erase operation, comprising single bit data loss in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss, wherein random single bit data loss is prevented in both the programming operation and the error operation.

35. (Amended) A method for [passivating] treating a non-volatile, electrically alterable semiconductor memory cell, thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a non-volatile, electrically alterable semiconductor memory cell comprising single bit data; and

exposing the memory cell to an atmosphere that comprises Hydrogen isotope by sputter deposition or pyrolytic diffusion, thereby reducing single bit data loss.

37. (Amended) A method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell having a programming operation and an erase operation, with a thermal oxide layer thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a silicon substrate and providing a memory cell, having a programming operation and an erase operation, the memory cell comprising single bit data;

defining source and drain regions in the silicon substrate and exposing the source and drain regions to an environment comprising Hydrogen isotope; and

growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss in the programming operation and the erase operation in the memory cell.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on August 22, 2002, and the references cited therewith.

Claims 1, 7, 26, 35, and 37; as a result, claims 1-2, 4-14, 26-32 and 35-39 remain pending in this application.

§103 Rejection of the Claims

Claims 1, 2, 4-14, 26-32, and 35-39 were rejected under 35 USC § 103(a) as being unpatentable over Admitted Prior Art in view of Lisenker et al. (WO 94/19829), Clark et al. (U.S. Patent No. 5,972,765) or Xiang et al. (U.S. Patent No. 6,218,245). The Examiner has introduced the reference of Xiang et al. The Xiang et al. reference is distinguishable from the claims of the present invention because Xiang does not describe FLASH memory and describes only one treatment with deuterium and does not describe a use of Hydrogen isotope in sputter deposition or pyrolytic diffusion as it applies to FLASH memory. As discussed in previous responses, the Lisenker and Clark references do not discuss FLASH memory at all.